Wavefront Sensing via High Speed DSP

ABSTRACT

Future light-weighted and segmented primary mirror systems require active optical control to maintain mirror positioning and figure to within nanometer tolerances. Current image-based wavefront sensing approaches rely on post-processing techniques to return an estimate of the aberrated optical wavefront with accuracies to the nanometer level. But the lag times between wavefront sensing, and then control, contributes to a significant latency in the wavefront sensing implementation. In this analysis we demonstrate accelerated image-based wavefront sensing performance using multiple digital signal processors (DSP's). The computational architecture is discussed as well as the heritage leading to the approach.

Scott Smith, Bruce Dean

{Jeffrey.S.Smith, Bruce.Dean}@nasa.gov

Optics Branch / 551 / NASA Goddard Space Flight Center

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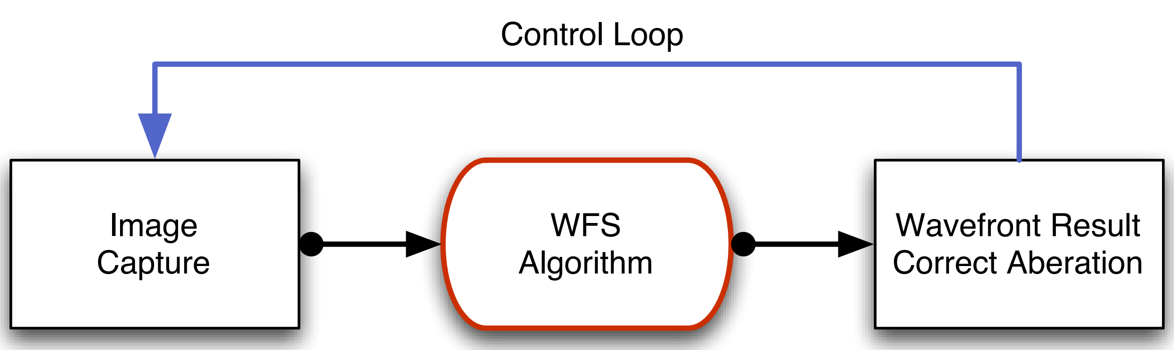
Background

- Technology development in the area of super-computing architectures for image-based wavefront sensing
- Goal: improve computational time for image based wavefront sensing performance by several orders of magnitude beyond the current state-of-the art
- Latency - an important limitation of image-based wavefront sensing is addressed



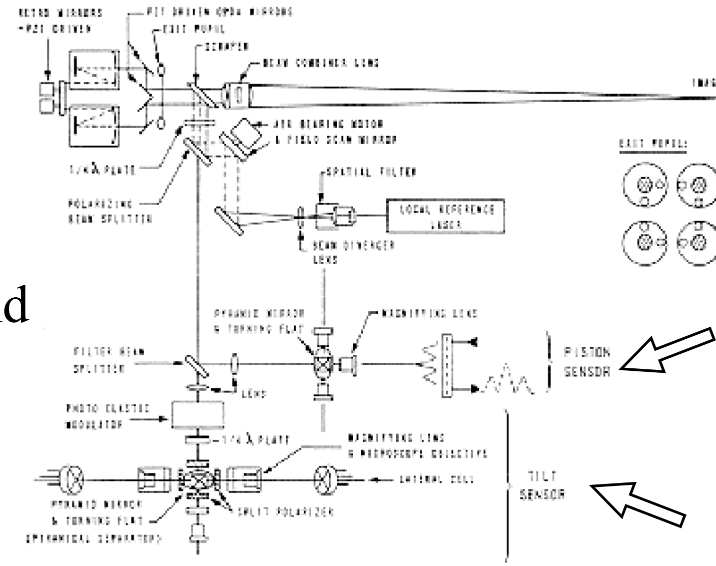
Background

- Supercomputing architectures
  - supercomputing hardware exists
  - computational architectures for image-based WFS do not exist
  - obtain theoretical computational performance of the Supercomputer
- NASA's priority list: - image-based WFS sensing will play a role in current & future NASA missions requiring optical correction and control.

Conventional Approach: e.g., Star-Fire Labs

- Interferometry; Shack-Hartmann,
- System complexity - increased cost and potential system failures,
- Expensive to maintain,
- Little bang for the buck – since Every degree of freedom requires a separate wavefront sensor.

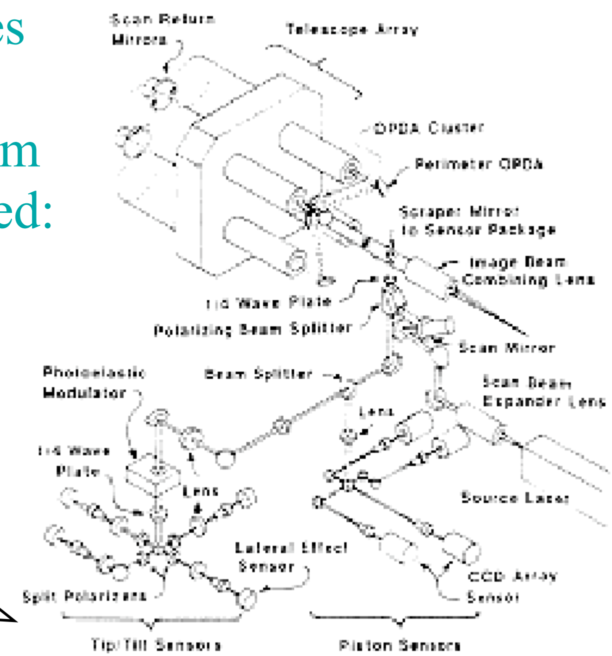
ADVANTAGE: these devices are analog and can provide near real-time monitoring of the wavefront.



Piston Sensor

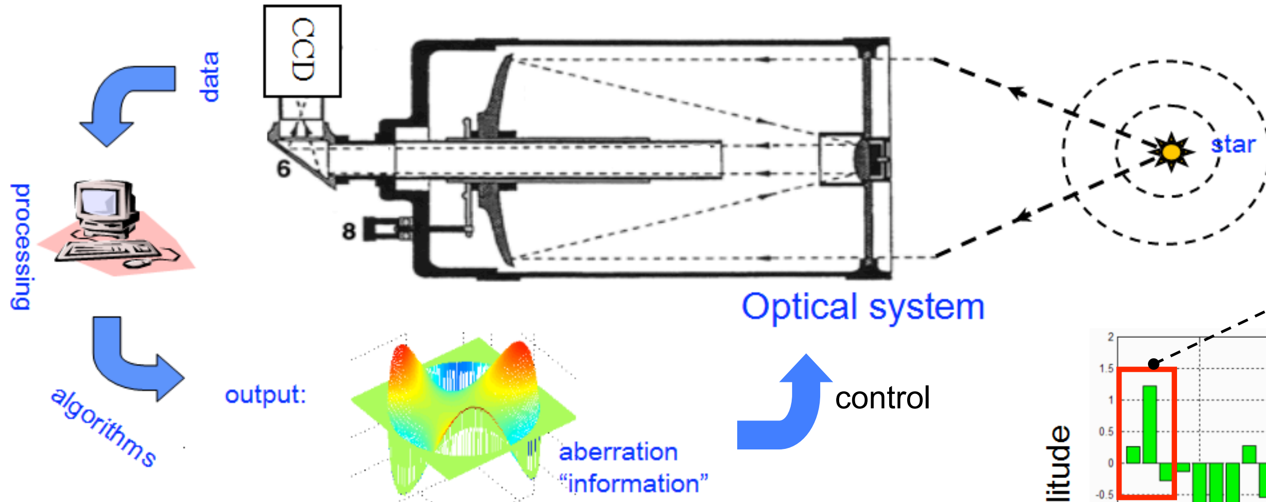
Tilt Sensor

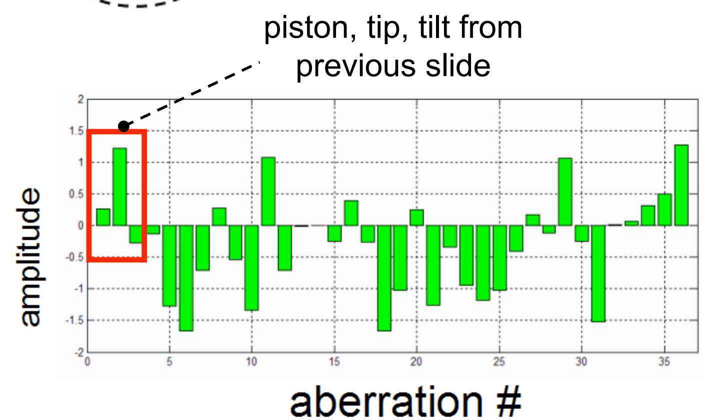
Only 3-degrees of freedom detected:



Tip Sensor

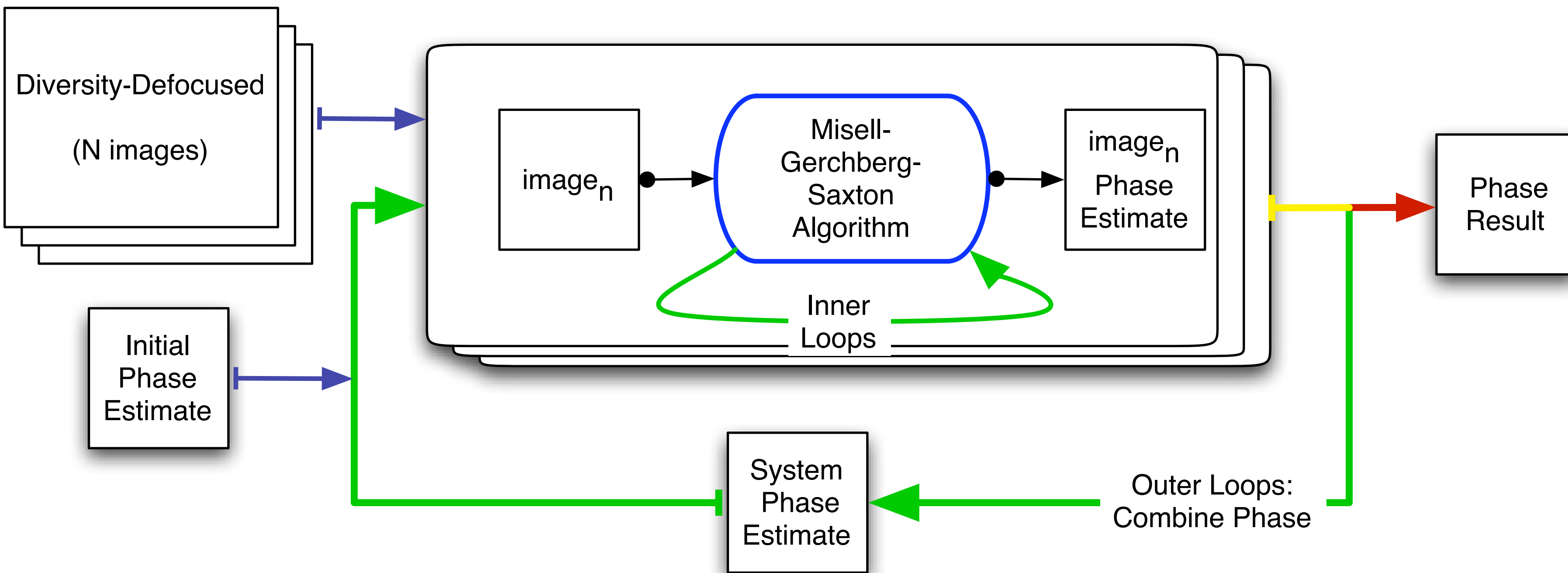
Image-Based Wavefront Sensing Concept:





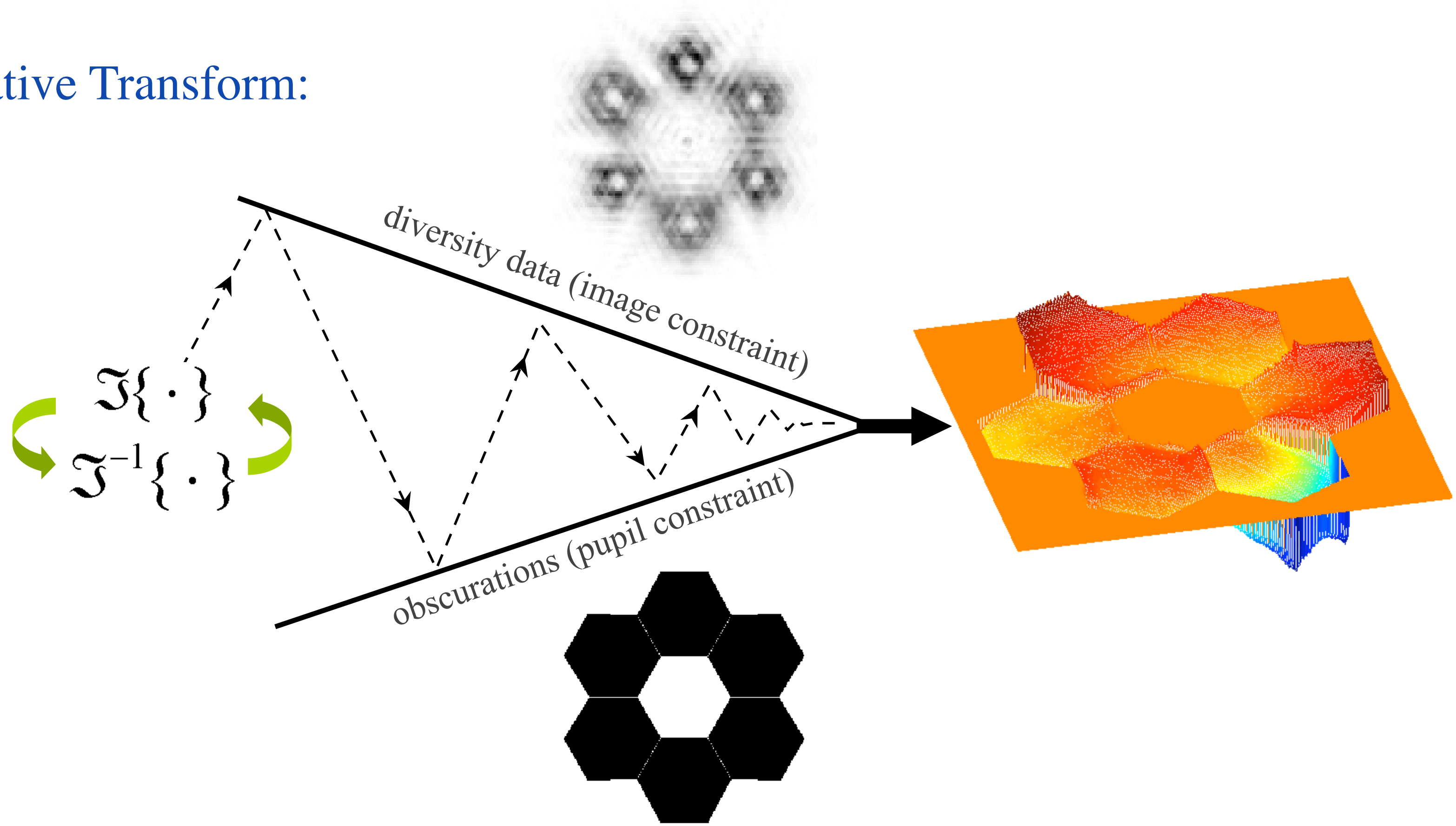
- Aberrations are detected out to arbitrary order,
- Basic Trade: optical hardware (conventional) / computational solution
- Significant delay - when the images are captured / wavefront is returned,
- Latency exists between "sensing" and the result (10's of minutes to hours).

Algorithm: Modified Misell-Gerchberg-Saxton



Core Algorithm Based on Iterative-Transform Approach – Fourier Transform Intensive:

Iterative Transform:



Solution - Reducing the Latency

- Parallel Processing
  - Multiple Processing Units
- Equivalent dedicated Supercomputer
- High bandwidth
- Supercomputer exist, but…
  - No dedicated solutions for wavefront sensing that properly exploit algorithm architecture.

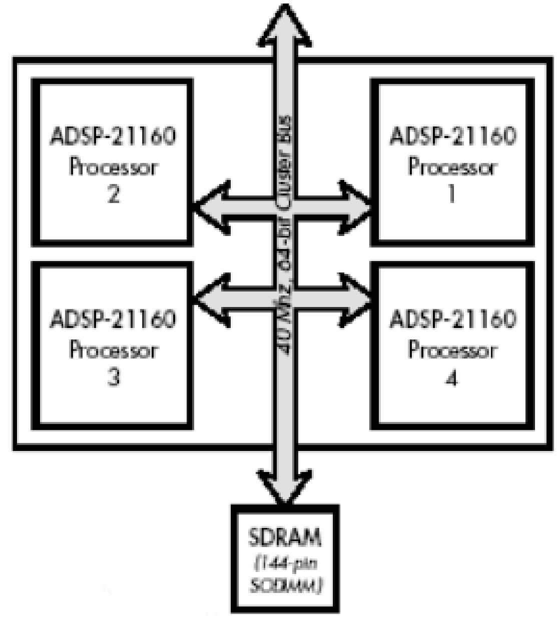
Digital Signal Processors (DSP)

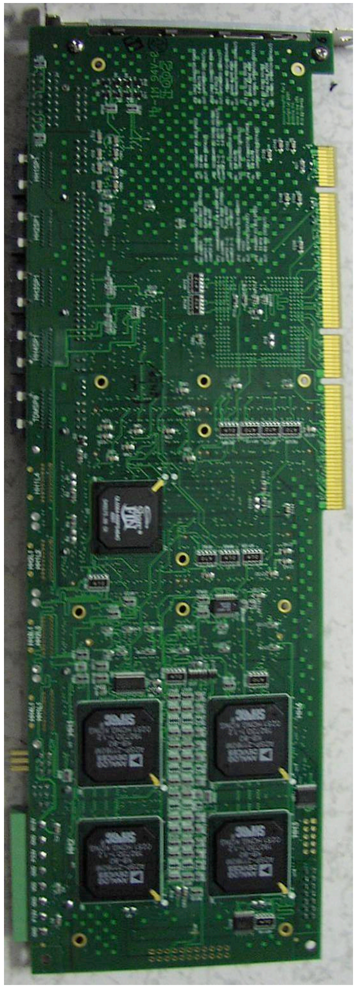
- **Desktop Processors**
  - Pentium
  - PowerPC
  - Good at most tasks
  - Multi-Tasking
  - General Purpose

- **DSP**
  - Great at scientific calculations
  - Great at FFT
  - Good at I/O
  - Low Power Rating

DSP Heritage - Hammerhead DSP Boards

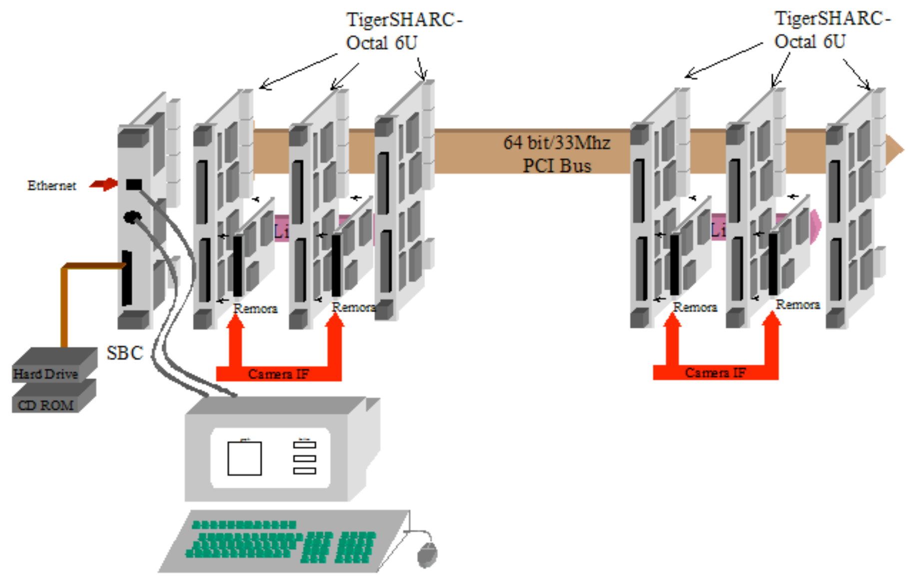
- Initial Implementation in 2003
- Four DSP's in right of lower image
- Factor of improvement over Single Pentium III
  - 4.2
- ADSP-21160 - 480 Mflops per DSP
- Demonstrated Proof of Concept: Showed that Algorithm performance is scalable with # of DSP's.





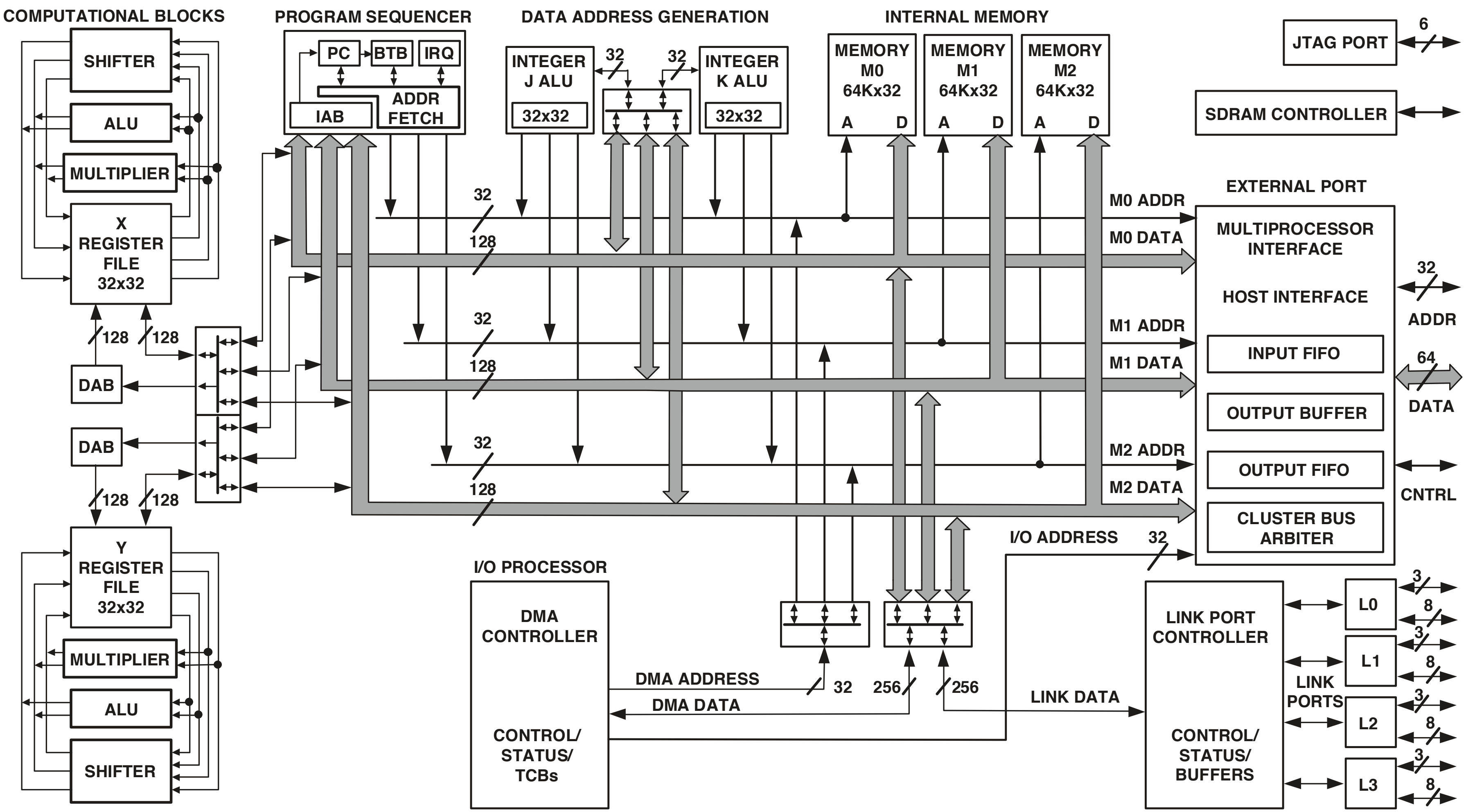
Analog Devices TigerSharc TS-101

- Harvard Architecture
  - Internal Memory, (No Cache)
  - Separate Data and Program Memory (4 and 2 Mbits each)
- Single Instruction Multiple Data (SIMD)
- Two Floating Point Cores
- 1.5 GFlops at 32 bit Single Precision
- 1 GB/sec of available I/O via link ports
- 3 Watts
- 250 MHz



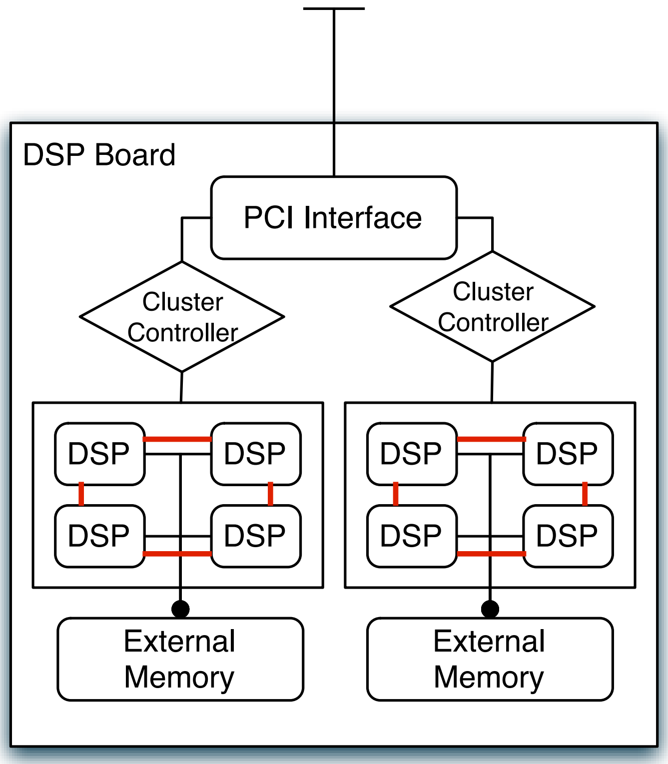
Analog Devices TigerSharc TS-101

FUNCTIONAL BLOCK DIAGRAM

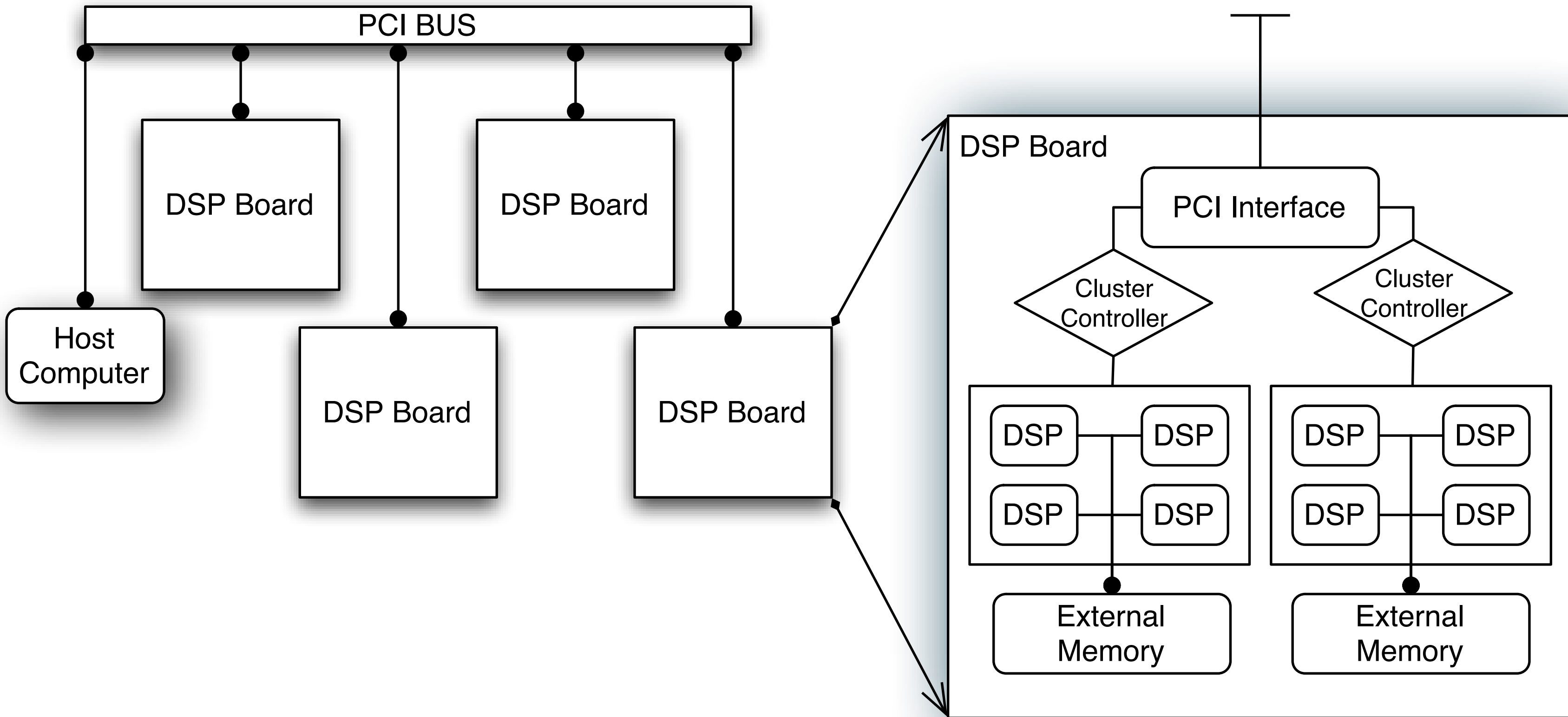


Architecture

- One DSP will not solve problem
- Connect multiple DSPs with interprocessor communication (Link Ports)
- Standard Cluster – 4 DSPs
  - Shared External Memory SDRAM
  - Read/Write internal memory
- Connect multiple clusters
- Host computer connected via PCI bus

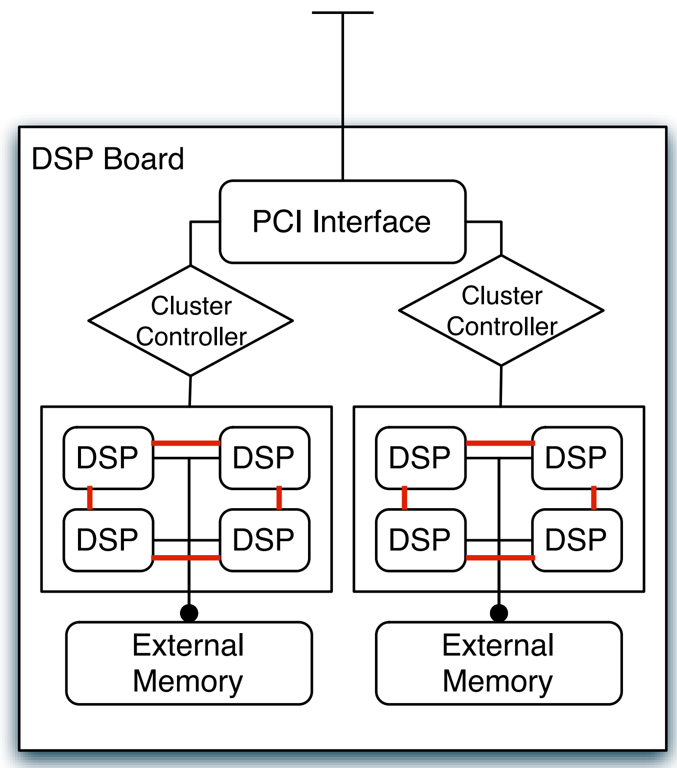


Architectural Block Diagram



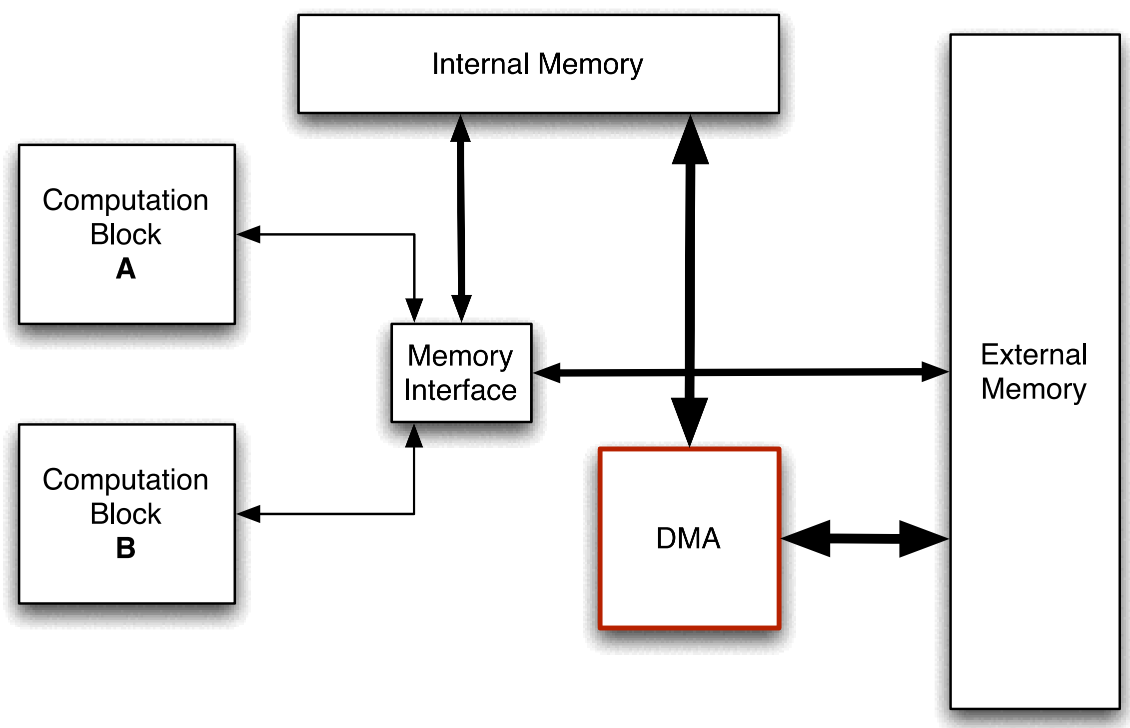
Step 1, Produce Results

- Disregard Timing
- Produce reliable wavefront data on DSPs
  - Start on 1 DSP
  - Transition to 4
-
- Bottlenecks on new architecture
  - External to Internal Memory movement
  - Data Downloading from Host Computer
  - Computations (FFTs)
    - Number of FFTs per DSP
    - Speed of each FFT



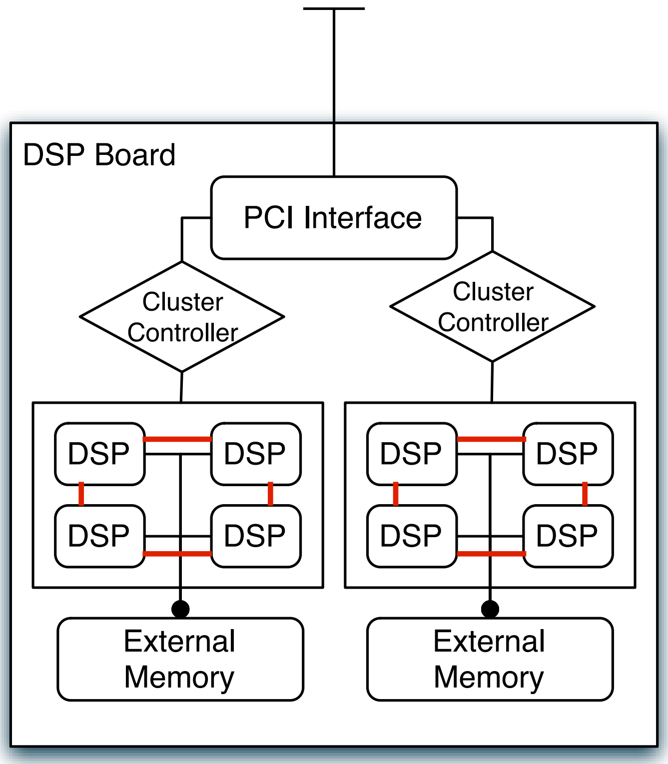
Direct Memory Access

- DMA
  - Allow movement of data without interrupting the core of the processor
  - Process Data Set 1 while acquiring Data Set 2
- Source and Destinations
  - Host computer
  - External shared memory
  - DSP internal memory
  - Link Ports



Multiple DSPs

- Based on timing for 1 Image on 1 DSP
  - Need more then 8 DSPs
  - Need more then 1 board
- Integrating Clusters and Boards
  - For each image Data only shared on 2-D FFT
  - For all images, Data shared on averaging the estimated phase



Reducing redundant work

- Optimize memory and FFTs for padding
  - Detector Image Size versus Pupil Image Size
- Downloading Constant Data outside control loop
  - System parameters don't change

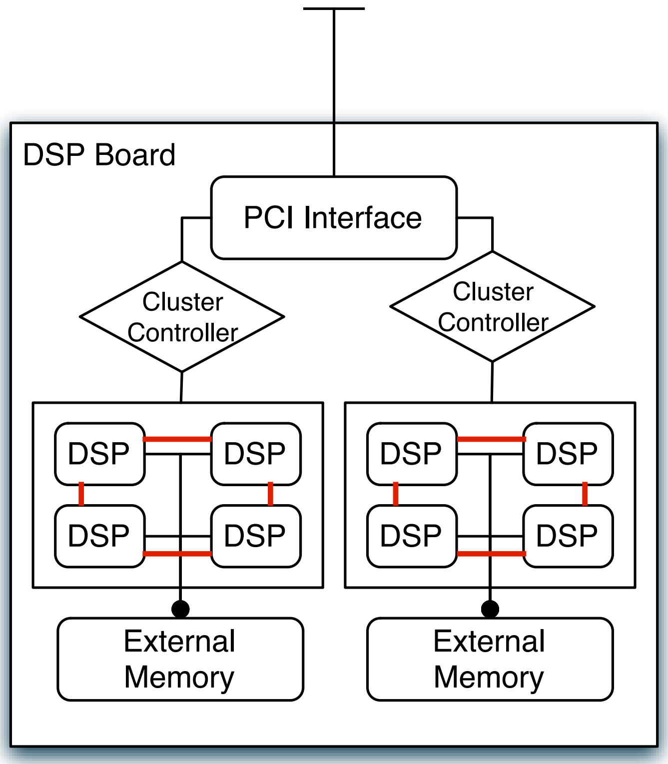
Optimized Library

- Decrease the time for each FFT

- TS-Lib for TigerSharc DSP
  - Floating Point Library optimized
  - Optimized for 1 DSP
  - Fastest available FFT
  - Fast Memory Movement (Simple)

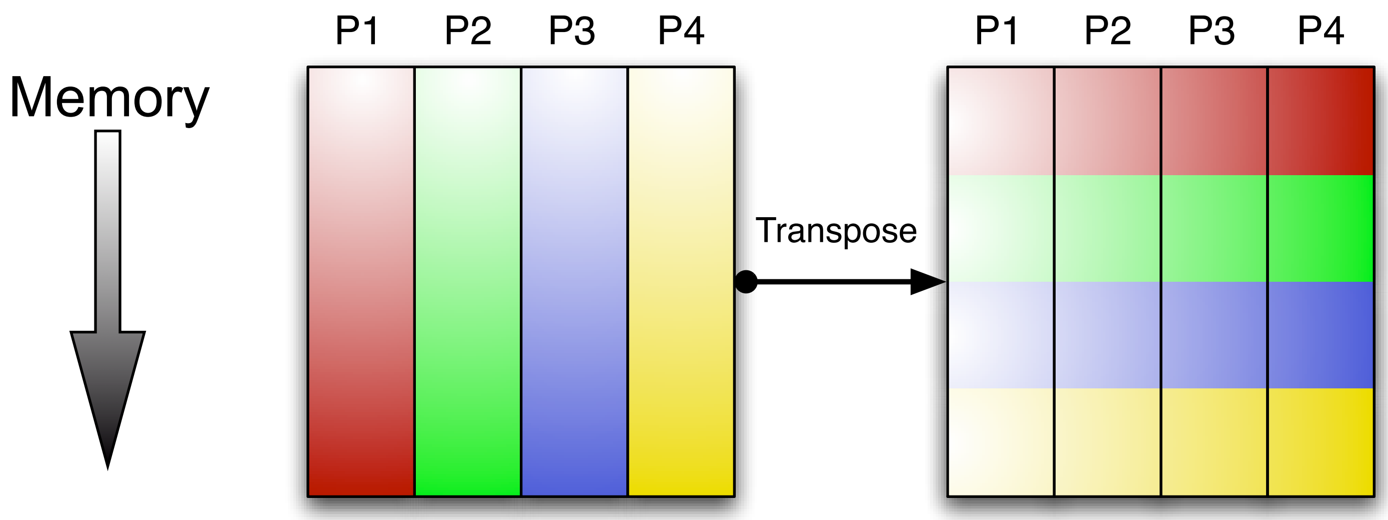
Decrease FFTs per DSP

- Increase number of DSPs
- Image FFT (2-D)
  - FFT each row
  - FFT result of each column
- Requires access to result
  - Data on each DSP must be moved to every other DSP



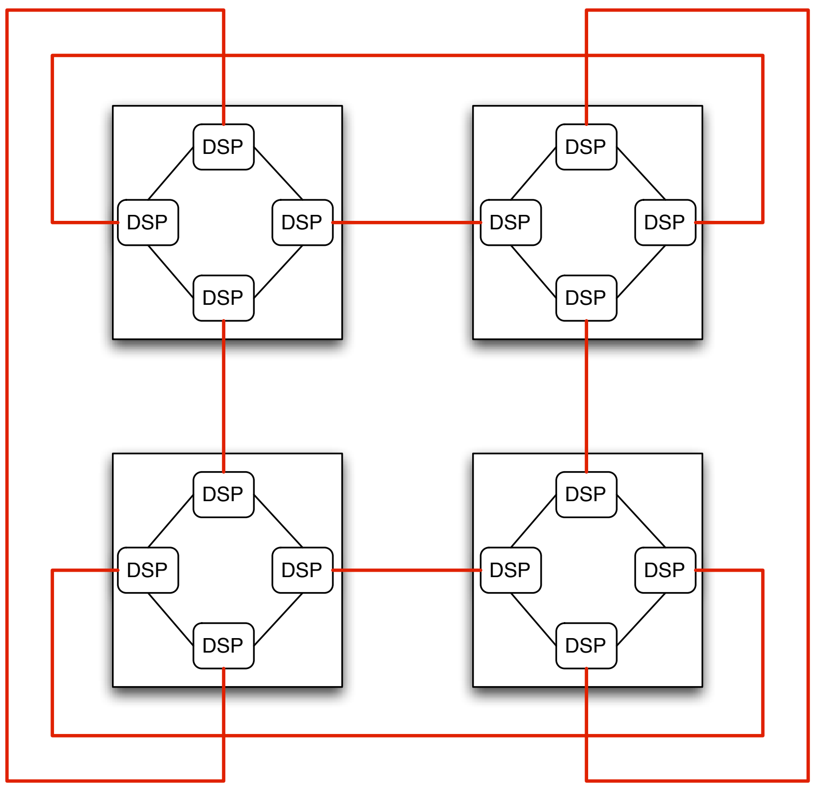
2-D FFT Transpose 1/2

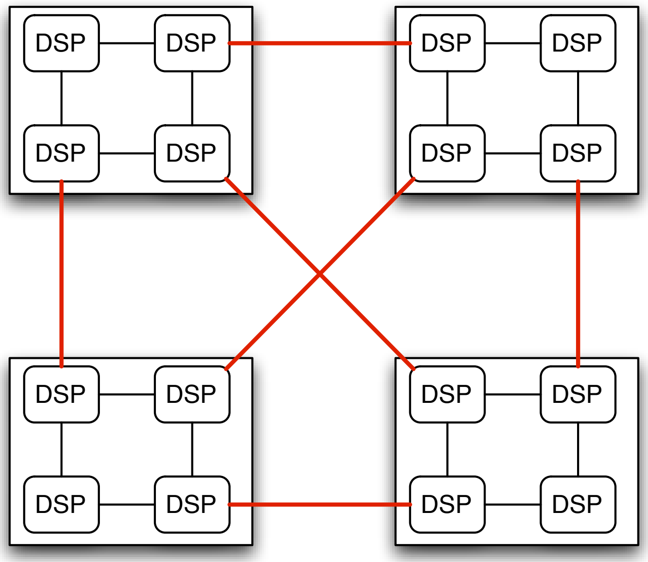
- Must be fast, because it happens twice per inner loop.
- Transpose over multiple Processors
  - Move data from each DSP to every other DSP



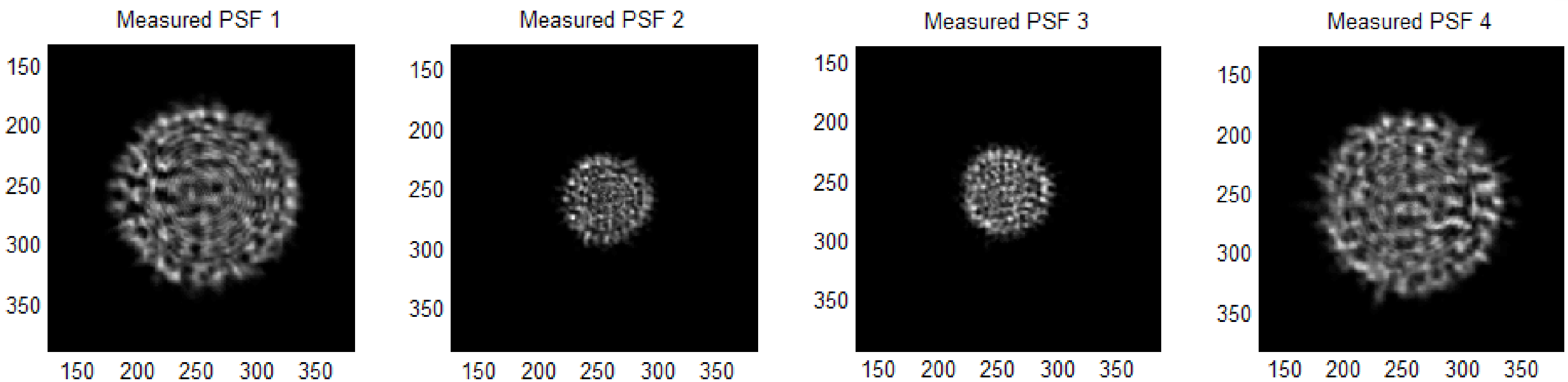
2-D FFT Transpose 2/2
Two Algorithms

- Single Stage
  - Each DSP transfers to every other DSP (link ports)
  - Faster theoretical
- Multiple Stage
  - Each DSP transposes on the cluster. (Shared Memory)
  - Then, Each cluster transposes (link ports)
  - One DSP “speaks” for its cluster to the other cluster
  - Faster in application





Experiment



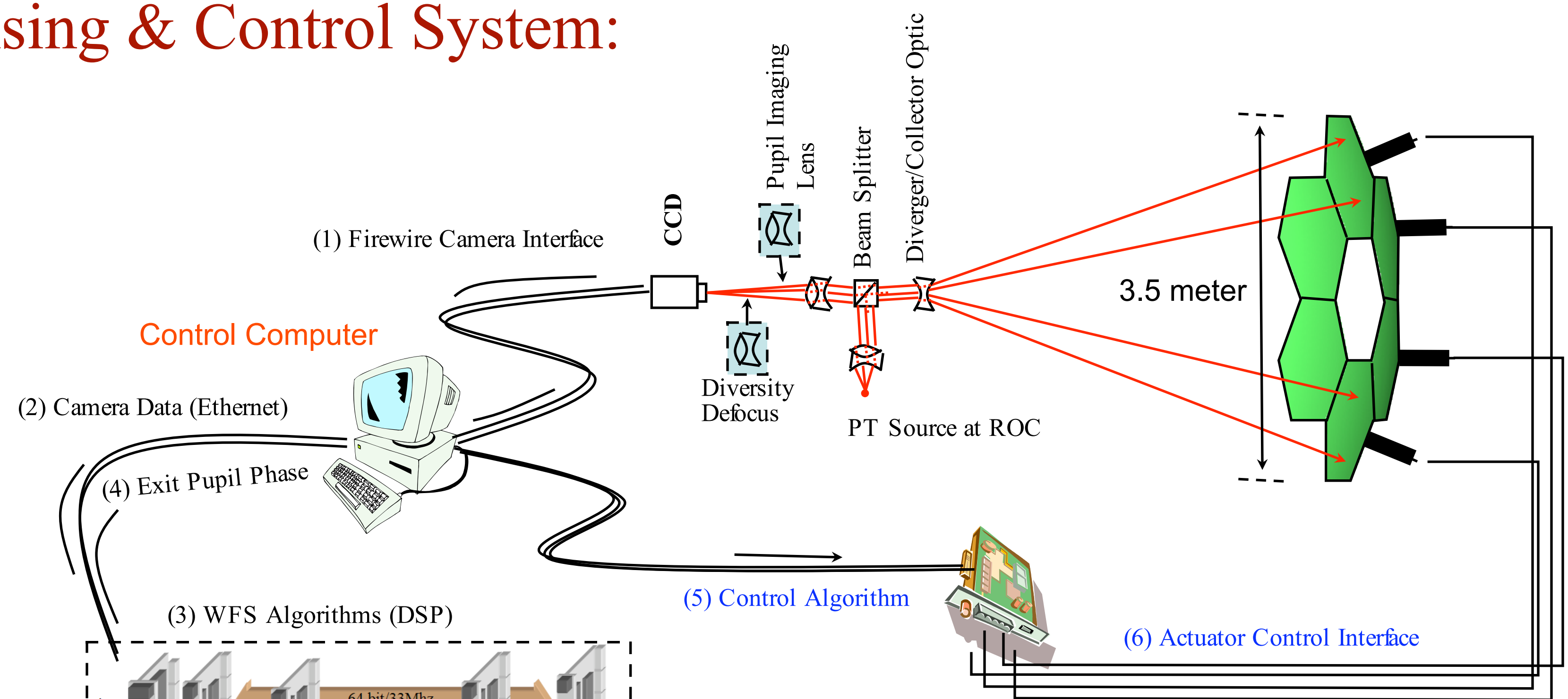
- 4 Diversity-Defocus images from GSFC's Wavefront Control Testbed (both + and (-) defocus shown)
- Detector: 16 bit, 512x512, 9μ pixels
- Pupil: 224x224
- 0^{O} Trefoil Introduced using Xinetics Deformable Mirror = .25 HeNe waves
- Other aberrations < .01
- Iterations: 5 inner loops, 25 outer loops, 95% Convergence

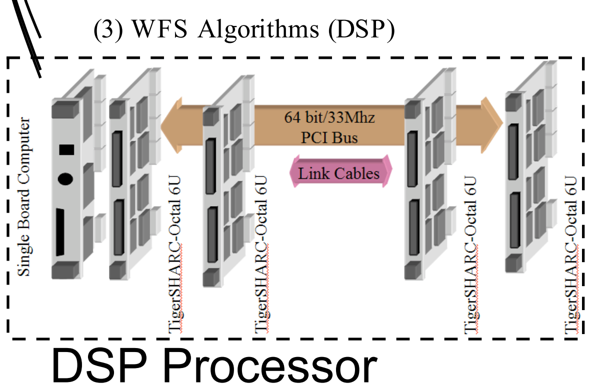
Speed Improvements

- Maltab Timing: 16.5 Minutes
  - Pentium IV at 3.0 GHz
- 16 DSP timing: 5.1 Seconds
  - 4 Images in serial
- 32 DSP timing: 2.6 Seconds
  - 2 Images in parallel
- Accuracy for 7 Significant Figures
- Factor of Improvement
  - 400

SPOT (Spherical Primary Optical Telescope) Wavefront Sensing & Control System:

NASA IR&D Proposal Funded in 2003





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- DSP becomes a server
  - Controlling a supercomputer with a laptop

Conclusions

- Lessons Learned
  - Matrix Transpose Algorithms
  - Scalability
- Next Steps
  - Removing the host computer
    - Images feed directly onto DSP
  - Implement each image in parallel
    - Add 32 more DSPs